11/3,K/35 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00576391 **Image available**
A DUAL-PORTED PIPELINED TWO LEVEL CACHE SYSTEM
SYSTEME ANTEMEMOIRE A DEUX NIVEAUX A STRUCTURE PIPELINE A DOUBLE PORT
Patent Applicant/Assignee:
INTEL CORPORATION,
Inventor(s):
FU John Wai Cheong,
MULLA Dean A,
MATHEWS Gregory S,
SAILER Stuart E,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200039764 A1 20000706 (WO 0039764)
Application: WO 99US31179 19991229 (PCT/WO US9931179)
Priority Application: US 98223847 19981231
Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ TZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 5299

Fulltext Availability:
Claims

Claim
... and
a queuing structure coupling the first level cache and the second level cache.

2 The cache memory of claim 1, wherein the first level **cache** and the second level cache are adapted to simultaneously receive a 64 bit virtual address at each one of the first and second address ports, respectively.

3 The cache memory of claim 2, wherein the first address port and the second address port for the second **level** cache simultaneously receive a first virtual address and a second virtual address.

4 The cache memory of claim 1, wherein the **first level** cache is adapted to contain only integer data, and wherein the **second level** cache is adapted to include integer and floating point data.
5 The cache memory of claim 1, wherein the first address port for the **first level** cache and the first address port for the **second level** cache are adapted to **simultaneously** receive a first virtual address, and wherein the **first level** cache and the **second level** cache are adapted to initiate a cache lookup for the first virtual address in a first clock cycle.

6 The cache memory of claim 5, wherein the **first** level cache memory is adapted to complete the cache lookup for the first virtual address in a first clock cycle, and wherein the queuing structure is adapted to signal a first level cache hit/miss for the first virtual address to the second level **cache** after a second clock cycle.
16
LI
:Suisudwoo Xiouiguioqovo diqo-uo oqj'Xiomaw oqoeo diqo-uo uv sllun uoilnoaxo jo loqumu -o
:Suisudiuoo di o...a first cache hit/miss signal corresponding to the first virtual address through a queuing structure to an arbitrator in the second level of the **cache** memory after a second processor clock cycle.

18 The method of claim 17, wherein providing a first cache hit/miss signal corresponding to the first...

ADDRESS IN A FIRST LEVEL OF SECOND VIRTUAL ADDRESS IN
THE CACHE MEMORY...

11/3,K/36 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00402970 **Image available**
A CACHE CONTROLLER WITH TABLE WALK LOGIC TIGHTLY COUPLED TO SECOND LEVEL ACCESS LOGIC
ORGANE DE COMMANDE D'ANTEMEMOIRE DOTE D'UNE LOGIQUE DE PARCOURS DE TABLE COUPLEE ETROITEMENT A UNE LOGIQUE D'ACCES DE SECOND NIVEAU
Patent Applicant/Assignee:
ADVANCED MICRO DEVICES INC,
Inventor(s):
PHARMA Puneet,
FAVOR John Gregory,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9743714 A1 19971120
Application: WO 97US8650 19970516 (PCT/WO US9708650)
Priority Application: US 96649847 19960516
Designated States: JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 9459

Fulltext Availability:
Detailed Description
Detailed Description
... walk logic after invoking the second level access logic (or vice versa), if an access request signal and a translate request signal are both received **simultaneously** or are pending **concurrently** .

The second level access logic also performs housekeeping functions, such as servicing a **snoop** request signal and flushing a table entry from the **second level** cache line to main memory.

In one embodiment, the two logics of the **second level** control unit are both formed on a single microprocessor chip that includes **two first level** caches: an instruction **cache** and a data **cache** . The instruction **cache** includes an instruction word **cache** that holds instructions and an instruction TLB that holds table entries for translation of instruction addresses. The data **cache** includes a data word **cache** that holds data operands and a data TLB that holds table entries for translation of data addresses. The two word caches and the two TLBs...

11/3,K/37 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00386800 **Image available**
METHOD AND CIRCUITRY FOR EXECUTING READ COMMANDS AND MODIFYING DATA WORDS IN A MULTI-LEVEL DISTRIBUTED DATA PROCESSING SYSTEM
PROCEDE ET CIRCUITS D'EXECUTION DE COMMANDES DE LECTURE ET DE MODIFICATION DE MOTS DE DONNEES DANS UN SYSTEME INFORMATIQUE DISTRIBUE MULTI-NIVEAUX
Patent Applicant/Assignee:
UNISYS CORPORATION,
Inventor(s):
CASTLE David Edgar,
DONLEY Greggory Douglas,
FLORA Laurence Paul,
MANOJ Manoj,

MASSONE Brian Joseph,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9727543 A1 19970731
Application: WO 97US1122 19970124 (PCT/WO US9701122)
Priority Application: US 96591843 19960125; US 96591844 19960125
Designated States: JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 11280
Fulltext Availability:
Detailed Description

English Abstract
A two port high level **cache** memory for use in a multi-level distributed data processing system includes: 1) a first tag-memory which receives READ commands through one port from a system bus; and 2) a second tag-memory which receives **READ** commands through another port from a processor bus. The two tag memories store identical sets of comparable addresses. With **two** tag memories the high **level** **cache** memory is able to respond immediately to two different **READ** commands which occur **concurrently** on the processor bus and the system bus. Also, a multi-level distributed data processing system includes: 1) a system bus (13) having a main memory (11) coupled thereto; 2) multiple high level **cache** memories (14), each of which has a first port coupled to the system bus (13) and a second port coupled to a respective processor bus ...

Detailed Description
... in the entire Pentium Pro system.

However, a problem which needs to be addressed in the above multi-level distributed data processing system is that **each** high **level** **cache** memory preferably should be able to respond quickly and **simultaneously** to two different **READ** commands, one of which occurs on a processor bus and the other of which occurs on the system bus. If the READ command on the processor bus is for a data word which is 5stored in the high level **cache** memory, then the high level **cache** memory preferably should present that data word on the processor bus quickly in order to enhance system performance. At the same time, if the READ...

11/3,K/38 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00358736 **Image available**
SYSTEM AND METHOD FOR PROCESSING MULTIPLE REQUESTS AND OUT OF ORDER RETURNS
SYSTEME ET PROCEDE DE TRAITEMENT DE DEMANDES MULTIPLES ET DE RETOURS DESORDONNES
Patent Applicant/Assignee:
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[redacted]:
NGUYEN Le Trong,
[redacted]WARA Yasuaki,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9641250 A2 19961219
Application: WO 96US8549 19960603 (PCT/WO US9608549)
Priority Application: US 95479035 19950607
Designated States: JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 8656

Fulltext Availability:
Detailed Description

Detailed Description
... READTWRITE port allows reading and writing of appropriate block-frame addresses in TAG RAM 302 and the

corresponding data in S-RAM 304, while the **READ** port allows **snooping** for
synchronizing multiple processor operations and bus coherency

FIG. 3 further depicts a **two - level** memory-hierarchy. As is well-known, the upper **cache** level allows quicker retrieval of data stored in the **cache** S-RAM 304 compared to the greater storage capacity but slower retrieval time of data stored in the main memory level in memory 112. Such...

11/3,K/39 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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0?57152 **Image available**
REDUCING CACHE SNOOPING OVERHEAD IN A MULTILEVEL CACHE SYSTEM WITH MULTIPLE BUS MASTERS AND A SHARED LEVEL TWO CACHE
REDUCTION DU TEMPS SYSTEME NECESSAIRE A L'ESPIONNAGE DES ACCES A L'ANTEMEMOIRE DANS UN SYSTEME D'ANTEMEMOIRE COMPORTANT PLUSIEURS BUS MAITRES ET UNE ANTEMEMOIRE PARTAGEE DE NIVEAU 2
Patent Applicant/Assignee:
ADVANCED MICRO DEVICES INC,
Inventor(s):
BOWLES James E,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9639666 A1 19961212
Application: WO 96US8592 19960604 (PCT/WO US9608592)
Priority Application: US 95462985 19950605
Designated States: JP KR AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 9079

Fulltext Availability:
Detailed Description
Claims

Detailed Description
... from the shared level 2 cache 30 to the first level I cache 20, as in step 207, the inclusion field in the shared level **cache** 30 is updated (to reflect that the first level 1 **cache** 25 now contains the tag-address corresponding to the required information), as in step 208, and the requested information is sent to the first bus master 10, as in step 209. The sending of the information from the shared **level 2 cache** 30 to the **first level** I **cache** 25 can be done **concurrently** with the sending of the information from the shared **level 2 cache** 30 to the first bus master 10 that made the memory **read** access

If a memory **read** access is made by a bus master that does not utilize the shared level 2 **cache** 30, such as the third bus master 55 as shown in Figure 1, then the procedure is a little different than that explained above. The...

Claim
... 2 cache to determine if said level 2 cache contains a tag-address that coincides with said
memory access address;
(1) if said level 2 **cache** does not contain any tag-address that coincides with said memory access address, obtaining said information corresponding to said memory access address from said main...for said one storage location within said level 2 cache indicates that said tag-address does not reside in any of said plurality of level **1** caches connected to said level **2** cache;
(1) said one of said level I caches copying said information
13
corresponding to said coincident tag-address from said **level 2** cache into an available one of said plurality of storage
locations within said one of said level I caches;

(2) said one of said **level** 1 caches sending said information residing
in said available one of said plurality of storage locations within said one of said **level** 1 caches to said one of said bus masters;
(3) said **level** 2 cache updating said inclusion field corresponding to said one of said plurality of storage locations within said **level** 2 cache which has said coincident tag-address stored therein to indicate that said one of said **level** 1 caches contains said coincident tag-address; (b) if said inclusion field for said one storage location within said **level** 2 **cache** indicates that said tag-address ... another of said level I caches sending said information corresponding to said coincident tag-address to said level 2 cache;
(2) said level 2 cache **retrieving** said information corresponding to said **coincident** tag-address from said another of said level I caches and copying said information into an available one
of said plurality of storage locations within said **one** **level** 2 cache;
(3) said one of said level I caches copying said information corresponding to said **coincident** tag-address from said **level** 2 cache into an available one of said plurality of storage locations within said one of said **level** 1 caches;
(4) said one of said level I caches sending said information corresponding to said **coincident** tag-address to said one of said bus masters; and
(5) said **level** 2 cache updating said inclusion field corresponding to said one of said plurality of storage locations within said level 2 **cache** to indicate that said one of said level I **caches** contains said coincident tag-address stored therein.

13. A method as in claim 12, comprising the further step of
(b) (...

11/3,K/40 **(Item 7 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00280307
CACHE SYSTEM AND METHOD FOR PREFETCHING OF DATA
SYSTEME D'ANTEMEMOIRE ET PROCEDE POUR LA PREEXTRACTION DE DONNEES
Patent Applicant/Assignee:
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Inventor(s):
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FARMWALD Michael P,
HAMPEL Craig,
KRISHNAMOHAN Karnamadakala,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9428485 A1 19941208
Application: WO 94US5340 19940516 (PCT/WO US9405340)
Priority Application: US 9369147 19930528
Designated States: AT AU BB BG BR BY CA CH CN CZ DE DK ES FI GB GE HU JP KG KP KR KZ LK LU LV MD MG MN MW NL NO NZ PL PT RO RU SD SE SI SK TJ TT UA UZ VN AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 9780
Fulltext Availability:
Claims

Claim
... output device
and the associated prefetch pointer is unmodified in main memory when a line of data is written by a processor device.

11 The **cache** memory system as set forth in claim 1, wherein the cache memory system comprises a first **level** cache and a

prefetching **second** **level** cache, said **second** **level** cache operating in
parallel with the **first** **level** cache between the requesting device and
main memory.

12 The cache memory system as set forth in claim 1,
wherein the cache memory system comprises a **first** **level** cache and a
prefetching **second** **level** cache, said **second** **level** cache operating in
series between the **first** level cache and main memory.
13 The cache memory system as set forth in claim 1,
wherein the prefetch pointer is stored in parity fields...

...prefetch pointer is stored in a region of main memory
separate from the line of data with which the prefetch pointer is
associated.

... The **cache** memory system as set forth in claim 13,
... ECC information is further stored in the parity fields located
... the line of data.

...is written by the processor.

59 The processing system as set forth in claim 48, wherein if
the prefetch pointer comprises a Null value, said **cache** controller
causing the next sequential line in memory to be prefetched.

60 The processing system as set forth in claim 48, wherein
the cache memory system comprises a first **level** cache and a
prefetching **second** **level** cache, said **second** **level** cache operating in
parallel with the **first** **level** cache between the processor and main
memory. - 45

61 The processing system as set forth in claim 48, wherein
the cache memory system comprises a **first** **level** cache and a
prefetching **second** **level** cache, said **second** **level** cache operating in
series between the **first** level cache and main memory.

62 The processing system as set forth in claim 48,
comprising an instruction cache for storing lines of data comprising
instructions and a data cache for storing lines of data comprising other
information requested, each **cache** maintaining independent prefetch
pointers.

63 The processing system as set forth in claim 48, wherein
the cache is adirect mapped cache.

64 The processing system...

11/3,K/41 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00196049 **Image available**
TWO-LEVEL BRANCH PREDICTION CACHE
ANTEMEMOIRE DE PREDICTION DE BRANCHEMENT A DEUX NIVEAUX
Patent Applicant/Assignee:
NEXGEN MICROSYSTEMS,
Inventor(s):
STILES David R,
FAVOR John G,
VAN DYKE Korbin S,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9113402 A1 19910905

Application: WO 91US826 19910206 (PCT/WO US9100826)
Priority Application: US 90306 19900226
Designated States: AT BE CH DE DE DK ES FR GB GB GR IT JP KR LU NL SE
Publication Language: English
Fulltext Word Count: 9090

Fulltext Availability:
Detailed Description

Detailed Description
... below to functional units will normally be understood to mean elements within CPU 10, not such external devices.

An Instruction Decoder (DEC) 12 performs instruction **fetch** , instruction decode, and pipeline control. DEC 12 optionally interleaves instruction **prefetch** of up to three **simultaneous** instruction streams. DEC 12 contains a **two - level** Branch Prediction **Cache** (BPC) 13. Ile BPC includes an integrated structure which contains dynamic branch history data, a physical branch target address, and a branch target buffer for each **cache** entry. As branch instructions are decoded, the BPC is consulted for information about that branch. Independent of the direction predicted, branches are executed in a...history bits, and 24 target instruction bytes with 3 target instruction valid (TIV) bits. Second level BPC 155 is a deep but narrow structure which **caches** only partial prediction information but for a much larger number of branch instructions. Second level BPC 155 contains 256 entries, each containing two bytes of partial target address information and one history bit.

In **parallel** with instruction decoding, the instruction's decode PC is used to perform **parallel lookups** in the first and **second level** BPCs. (Since the incoming instructions have not been decoded at this point, non-branch instructions are also **checked**). In the event of a hit on **first level** BPC 152, the target instruction bytes are communicated to instruction decoder 160, the branch history bits are communicated to IDC 162, and the target address...bad address prediction is no worse than no prediction. Further, the occurrence of such bad predictions corresponds to the miss rate of the second level **cache** and thus is reasonably low given the relatively large number of cache entries. This is also enhanced by applying the hardware savings from eliminating the tag storage to increasing the number of cache entries.

Operation
A first level cache size of 36 entries and **second level** cache size of 256 entries, in combination with a factor of 16 difference in per-entry cost, results in second-to- **first level** cache ratios of eight times the number of entries, yet still almost half the size. With this much larger size, even given the direct-mapped organization, the **second level** cache provides an effective backup to the **first level** cache.

As each branch instruction is fetched its address is used to perform parallel look-ups in the two levels of BPC: the large-set or fully associative **first level** access using the full branch address; and the direct-mapped, tag-less **second level** using only a subset of the address bits for the index.
If there is a tag match with a **first level** cache entry, then all of this entry's prediction information is read out, and the **second level** BPC is ignored. All the necessary predictions are made, effectively eliminating or hiding any delays in otherwise processing the branch instruction and in starting processing...

11/3,K/42 **(Item 9 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT

J0174287
ARITHMETIC UNIT
UNITE ARITHMETIQUE

Patent Applicant/Assignee:
WANG LABORATORIES INC,
Inventor(s):
ZUK William S,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9007745 A1 19900712
Application: WO 89US5710 19891220 (PCT/WO US8905710)
Priority Application: US 88817 19881229
Designated States: AT AU BE CH DE ES FR GB IT JP LU NL SE
Publication Language: English
Fulltext Word Count: 13400

Fulltext Availability:
Detailed Description

Detailed Description
... number of cache read or write operations in conjunction with the AU 10. As has been previously mentioned, the AU 10 determines the number of **cache** read or write cycles required for a particular operand as a function of the operand alignment, as indicated by VA<29:31>, and the length of the operand, as indicated by bits 8-15 of IRO as stored in **L1 / L2** 98, The AU 10 also provides this information to CP 12 such that both units operate **in tandem** to **read** operands and store results in the CP 12 **cache** memory, This aspect of the invention will be further discussed below in relation to the flow chart of Fig. 5d,
For unconditional branch type operations...

11/3,K/43 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00126481
INTERLEAVED SET-ASSOCIATIVE MEMORY
MEMOIRE ENTRELACEE A ASSOCIATION D'ENSEMBLES
Patent Applicant/Assignee:
AMERICAN TELEPHONE & TELEGRAPH COMPANY,
Inventor(s):
PATRICK David Michael,
Patent and Priority Information (Country, Number, Date):
Patent: WO 8504737 A1 19851024
Application: WO 85US539 19850329 (PCT/WO US8500539)
Priority Application: US 84644 19840411
Designated States: AT BE CH DE FR GB IT LU NL SE
Publication Language: English
Fulltext Word Count: 8322

Abstract
... the memory parts and each of the cache sets. The cache receives a word over the bus in two pairs of contiguous words. The **cache** memory is updated with both words of a word pair simultaneously. The pairs of words are each stored simultaneously into locations of one of either of the **cache** sets, each word into a location of a different memory part and of a **different level** . **Cache** hit **check** is performed on all locations of a level **simultaneously** . All locations of the **checked** level are accessed **simultaneously** , and the **cache** hit **check** is performed on all locations of the checked level simultaneously.